REMARKS

This is in response to the Office Action mailed on October 21, 2004, and the references cited therewith.

Claim 1, 10-13, 15, 19, 20, and 25-27 have been amended; as a result claims 1-5, 7-13, 15-17, 19, 20 and 24-27 are now pending in this application.

§103 Rejection of the Claims

Claims 1, 2, 4, 7-13, 15, 17, 19, 20 and 24-27 were rejected under 35 USC § 103(a) as being unpatentable over U.S. 6,289,369 (hereinafter Sundaresan) in view of U.S. 6,658,447 (hereinafter Cota-Robles).

Applicants respectfully submit that claims 1, 2, 4, 7-13, 15, 17, 19, 20 and 24-27 should not be rejected under 35 U.S.C. § 103 for the reason that prior art references when combined do not teach or suggest all of the claim limitations of the independent claims of the present application.

To establish a **prima facie** case of **obviousness**, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

EMPLOYING SYMMETRIC MULTIPROCESSORS

Claim 1 includes the following limitation:

the distributing the of <u>task</u> to the available thread being responsive to dynamically assigning a new priority to the <u>task</u>;....

The Office Action, in rejecting claim 1, contends that the above limitation is anticipated by the following disclosure in Cota-Robles:

Referring now to FIG. 3B, there is shown a more detailed flowchart of an embodiment of method 300 implemented by SMT processor 100 in accordance with the present invention. ...

Once dynamic priorities have been determined, the processor selects 334 instructions for processing on the next clock cycle according to the determined dynamic priorities. These instructions are transferred 338 to the processor pipeline and the process is repeated for the next clock cycle.

Cota-Robles, Col. 12, lines 50-67.

The above quote from Cota-Robles describes a simultaneous multithreading (SMT) processor that selects instructions for processing. The selection of instructions corresponds to the selection of threads that have already been scheduled on the processor (Abstract). The processor selects the threads according to determined dynamic priorities and the processor pipeline receives the instructions for execution on the processor. The above described process repeats for each clock cycle.

An SMT processor allows multiple threads to execute on a single processor.

Simultaneous multithreading (SMT) processors allow threads from multiple hardware contexts to execute simultaneously on <u>a single processor</u>. The OS schedules multiple threads onto an SMT processor, and on each clock cycle, the SMT processor selects instructions for execution from among the scheduled threads.

Cota-Robles, Col. 2, lines 1-2.

Claim 1 requires distributing a task to an available thread responsive to dynamically assigning a new priority to the <u>task</u>. Merely, for example, a task scheduler may distribute a task from a task queue to a thread, the distribution to the thread responsive to dynamically assigning a new priority to the task. In contrast, the above quote from Cota-Robles does not describe the distribution of a task to an available thread responsive to dynamically assigning a new priority to the task; but rather, the selection of a thread according to determined dynamic priorities. The Office Action points out that "sections in Cota-Robles that describe the instruction and the threads...could be interpreted as the Applicant's claimed thread and tasks." Applicants respectfully point out that the "task" of claim 1 is different from the "thread" of the above quote from Cota-Robles in more than name only. Specifically the "task" of claim 1 is distributed from a task queue to a thread that, in turn, is assigned to any one of multiple processors whereas the "threads" from the above quote from Cota-Robles have already been assigned to a single processor. Indeed, Cota-Robles does not describe dynamically assigning a new priority to a task that may be assigned to any one of multiple processors in a multiprocessor system, as required by claim 1; but rather, Cota-Robles describes allowing threads from multiple hardware contexts to execute simultaneously on a single processor because Cota-Robles describes an invention that utilizes SMT processor architecture (Col. 2, line 55), as described above (Col. 2, lines 1-2). Clearly, a "task" cannot be equated to a "thread" for at least the reason provided above. Cota-Robles therefore cannot be said to anticipate the above quoted limitation because Cota-Robles discloses the selection of a thread that has already been assigned to a <u>single</u> processor, according to determined dynamic priorities, and claim 1 requires distributing a task to an available thread that is assigned to any one of multiple

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processors within a multiprocessor system, the distributing the "<u>task</u>" responsive to dynamically assigning a new priority to the "<u>task</u>."

Independent claim 9 includes a limitation corresponding substantially to the above-discussed limitation of claim 1. The above remarks are accordingly also applicable to a consideration of these independent claims.

In addition, if an independent claim is nonobvious under 35 U.S.C. § 103 then, any claim depending therefrom is nonobvious and rejection of claims 2, 4, 7-8, 10-13, 15, 17, 19, 20 and 24-27 under 35 U.S.C. § 103 is also addressed by the above remarks.

Claims 3 and 16 were rejected under 35 USC § 103(a) as being unpatentable over Sundaresan in view of Cota-Robles in further view of U.S. Patent No. 6,314,089 (hereinafter Szlam).

Claims 3 and 16 depend on independent claims 1 and 9 respectively. If an independent claim is nonobvious under 35 U.S.C. § 103 then, any claim depending therefrom is nonobvious and rejection of claims 3 and 16 under 35 U.S.C. § 103 is also addressed by the above remarks.

Claims 5 was rejected under 35 USC § 103(a) as being unpatentable over Sundaresan in view of Cota-Robles in further view of U.S. Patent No. 6,222,530 (hereinafter Sequeira).

Claims 5 depends on independent claim 1. If an independent claim is nonobvious under 35 U.S.C. § 103 then, any claim depending therefrom is nonobvious and rejection of claim 5 under 35 U.S.C. § 103 is also addressed by the above remarks.

In summary, Sundaresan in combination with Cota-Robles combination with Szlam in combination Sequeira does not teach or suggest each and every limitation of Title: METHODS AND APPARATUS FOR EXECUTING A TRANSACTION TASK WITHIN A TRANSACTION PROCESSING SYSTEM EMPLOYING SYMMETRIC MULTIPROCESSORS

claims 1 and 9 as required to support rejections of the independent claims of the present application under 35 U.S.C.§ 103.

In summary, Applicants believe that all rejections presented in the Final Office Action have been fully addressed and withdrawal of these rejections is respectfully requested. Applicants are mindful that the proposed amendment cannot, as a matter of right, be entered. Nonetheless, Applicants believe that the proposed amendment requires only a cursory review by the Examiner to remove issues from appeal. Applicants furthermore believe that all claims are now in a condition for allowance, which is earnestly solicited.

Serial Number: 09/320,252 Filing Date: May 26, 1999

Title: METHODS AND APPARATUS FOR EXECUTING A TRANSACTION TASK WITHIN A TRANSACTION PROCESSING SYSTEM

EMPLOYING SYMMETRIC MULTIPROCESSORS

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney at 408-846-8871 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 21st day of <u>January</u>, 2005.

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